REMARKS

In this response, no claims have been added or canceled. Thus, claims 1-9, 12-15, 17, 22-67, 69-74, 76-85 remain pending. The Office Action issued by the Examiner has been carefully considered by Applicant.

Claims 1-9, 12-15, 22-67, 69-74, 76-77 and 85 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (hereinafter, "Jones") (U.S. Patent No. 6,430,164) in view of Lu et al. (hereinafter, "Lu") (U.S. Patent No. 5,734,699).

The Examiner previously cited Lu as a secondary reference in an attempt to provide a prima facie case in which Lu supports the teaching of a real-time interface processor (RTIP) and an application processor, wherein the "RTIP performs real-time operations" and the "application processor performs high level processing functions" as recited in Applicant's independent claim 1. In this Office Action, the Examiner continues to rely upon the real time processor 554 of Lu as teaching a "real-time interface processor" as recited by Applicant. The Examiner describes Lu's real time processor 554 as processing real-time information and communicating control information over VME bus 520 (see Office Action p. 4 and Lu Fig. 9). The Examiner further describes Lu's processor 554 as being coupled to VME bus 520 to facilitate/perform processing (see Office Action p. 28 in Response to Arguments).

If, for the sake of argument, it is accepted that Lu's processor 554 teaches a real-time interface processor, then the Examiner has not stated or made clear what Lu teaches to be an "application processor" of the gateway node as recited by Applicant's claim 1. When referring to Lu's Fig. 9, the text sections of Lu cited by the Examiner describe real-time processor 554 and several DSPs (557, 559, 561, 563) in parallel. The cited sections describe that real-time processor 554 controls the operation of the parallel DSPs to handle inbound and outbound TDM radio traffic. There are no other processors in Lu's Fig. 9

referred to by the Examiner in the remainder of the Office Action. Thus, it must be that the Examiner asserts that one of the DSPs is an "application processor" recited by Applicant's claim 1.

However, as Applicant made clear previously, Applicant's independent claim 1 recites "the at least one application processor performs high level processing functions". A person of skill in the art would understand Lu's DSPs in Fig. 9 as teaching the processing of real time inbound and outbound radio traffic, and thus teaching away from "high level processing". The Examiner fails to make any argument at all relating the operation of the DSPs to "high level processing functions" as recited by Applicant.

Applicant's independent claim 77 is also believed allowable for the above reasons and further recites that "the at least one RTIP is coupled between the at least one interface port and the at least one application processor." The Examiner will recall that claim 77 was newly added in Applicant's last response. However, in making the current rejection of claim 77, the Examiner has failed to even address or make argument with respect to this limitation.

Instead, the Examiner's current rejection of claim 77 is identical to the rejection made in the prior Office Action, although the foregoing claim recitation does not appear in Applicant's claim 1. Accordingly, Applicant respectfully submits that a prima facie case is not presented for claim 77, and respectfully requests that the present Office Action be re-mailed with appropriate added Examiner argument and a new time period for response so that Applicant may properly and fully understand the Examiner's position prior to appeal. This situation is believed to similarly exist for Applicant's independent claim 85.

Applicant's dependent claim 78 recites that "data is collected by the gateway node using the at least one interface port". According to the Examiner's argument that Lu's real time processor 554 is an "RTIP", the Examiner must be taking the position that the coupling to VME bus 520 by processor 554 in Lu's Fig. 9 is the "at least one interface

port" recited by Applicant. However, claim 78 further recites that "the at least one RTIP performs processing to route the data to one of the plurality of network elements". Lu describes that control information is received by processor 554 from VME bus 520 to control the operation of the parallel DSPs (col. 21: lines 54-60). The Examiner fails to argue how both this control information is "collected by the gateway node" and that processor 554 "performs processing to route the data" (emphasis added) as recited by Applicant's claim 78. Instead, Lu only describes processor 554 as using the control information to control the operation of the parallel DSPs. Lu further teaches that inbound radio traffic is processed by the parallel DSPs and sent over TDM bus 522, but this radio traffic is not collected from VME bus 520 through processor 554.

Applicant's claim 81 recites that "the at least one application processor hosts an application associated with the bus". The Examiner again cites the identical section of Lu used above (this is the only section of Lu cited through the entire Office Action). The cited section of Lu, as discussed previously, teaches a real-time processor 554 controlling a group of parallel DSPs handling inbound and outbound radio traffic. There is no mention by Lu in the cited section that one of the DSPs hosts an application associated with the bus. Instead, the DSPs are only described here by Lu as processing TDM time slots.

Applicant's claim 82 recites that "the at least one RTIP passes IP packets through the gateway node under control of the at least one peripheral electronic device". The rejection made by the Examiner cites the wrong wording from the claim, and thus the Examiner fails to make a prima facie rejection for this claim. It should be further noted that the cited section of Lu (the same cited section as used above) only describes the real-time processor 554 as controlling the processing of inbound and outbound radio information. Also, a person of skill in the art would read Lu as teaching that the parallel DSPs pass information through the gateway node, rather than the real-time processor 554, which Lu describes as controlling the parallel DSPs. Finally, the Examiner has not

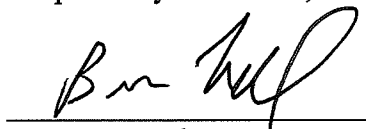
identified any peripheral electronic device as controlling passing of packets as recited in claim 82.

Applicant's claim 83 recites that "the at least one application processor is operable to access raw data from the at least one RTIP". The Examiner again cites the same section of Lu, which describes that real-time processor 554 controls the parallel DSPs. The Examiner fails to make any argument as to why one of skill in the art would consider any of the DSPs to be accessing "raw data" from the real-time processor 554.

Applicant's claim 84 recites that "the real-time operations of the at least one RTIP run below an operating system executed on the at least one application processor". The Examiner again cites the same section of Lu, which describes real-time processor 554 as controlling the parallel DSPs. The Examiner does not provide any argument as to why one of skill in the art would consider processor 554 to "run below an operating system executed" on any of the DSPs, which Applicant understands the Examiner to be asserting as showing an application processor of the gateway node, when it is processor 554 that Lu describes as being the controlling processor.

In view of the above, Applicant respectfully requests reconsideration of this application and the allowance of all pending claims. It is respectfully submitted that the Examiner's rejections have been successfully traversed and that the application is now in order for allowance. Applicant believes that the Examiner's other arguments not discussed above are moot in light of the above arguments, but reserves the later right to address these arguments. Accordingly, reconsideration of the application and allowance thereof is courteously solicited.

Respectfully submitted,



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Bruce T. Neel
Reg. No. 37,406

Customer Number 33717
GREENBERG TRAURIG, LLP
2450 Colorado Avenue, Suite 400E
Santa Monica, CA 90404
Phone: (602) 445-8339
Fax: (602) 445-8100
E-mail: neelb@gtlaw.com